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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/049,207	06/14/2002	Makoto. Okazaki	MTS-3307US	8093
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Ratner & Prestia		HUBER, PAUL W		
Suite 301 One Westlakes Berwyn				
P O Box 980		ART UNIT		
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Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 10/049,207	Applicant(s) OKAZAKI ET AL.	
	Examiner Paul Huber	Art Unit 2653	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 12 May 2005.  
 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.  
 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-28 is/are pending in the application.  
 4a) Of the above claim(s) 9-17, 18/9-17, 21-23 and 26-28 is/are withdrawn from consideration.  
 5) ☒ Claim(s) 8 is/are allowed.  
 6) ☒ Claim(s) 1-7, 18/1-7, 19, 20, 24 and 25 is/are rejected.  
 7) ☒ Claim(s) 18/8, 19, 20, 24 and 25 is/are objected to.  
 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.  
 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) ☒ All b) ☐ Some \* c) ☐ None of:  
 1. ☐ Certified copies of the priority documents have been received.  
 2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
 \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

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The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The title should be amended to be specific to the elected claims.

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Applicant's election without traverse of Group I, claims 1-8, 18/1-8, 19, 20, 24 & 25, in the reply filed on May 12, 2005 is acknowledged.

Claims 19, 20, 24 and 25 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The program/medium of claims 19, 20, 24 and 25 could be infringed without infringing upon the respective base claims drawn to a buffer memory address translation device. Possession of a program/medium that infringes on the claimed program/medium does not necessarily mean that one has possession of the actual buffer memory address translation device and therefore the device of the base claim is not necessarily infringed. Hence, claims 19, 20, 24 and 25 are improper dependent claims as failing the Infringement test outlined in **MPEP 608.01(n) II. TREATMENT OF IMPROPER DEPENDENT CLAIMS, III. INFRINGEMENT TEST.**

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 19, 20, 24 and 25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, a person of skill in the art must be able to ascertain the metes and bounds of the claimed invention, i.e., the claimed program, per se, or the claimed program embodied on a computer readable medium. The claimed program does not particularly point out and distinctly claim how the computer is to function in a particular fashion, but rather instead recites limitations pertaining to the elements of the buffer memory address translation device which are not defining of the program.

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The following is a quotation of the appropriate paragraphs of 35 U.S.C. 101 that form that basis for the rejections under this section made in this Office action:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 24 and 25 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 24 and 25 are drawn to a "program" *per se* as recited in the preamble and as such is non-statutory subject matter. See MPEP § 2106.IV.B.1.a. Data structures not claimed as embodied in computer readable media are descriptive material *per se* and are not statutory because they are not capable of causing functional change in the computer. See, e.g., *Warmerdam*, 33 F.3d at 1361, 31 USPQ2d at 1760 (claim to a data structure *per se* held nonstatutory). Such claimed data structures do not define any structural and functional interrelationships between the data structure and other claimed aspects of the invention, which permit the data structure's functionality to be realized. In contrast, a claimed computer readable medium encoded with a data structure defines structural and functional interrelationships between the data structure and the computer software and hardware components which permit the data structure's functionality to be realized, and is thus statutory. Similarly, computer programs claimed as computer listings *per se*, i.e., the descriptions or expressions of the programs are not physical "things." They are neither computer components nor statutory processes, as they are not "acts" being performed. Such claimed computer programs do not define any structural and functional interrelationships between the computer program and other claimed elements of a computer, which permit the computer program's functionality to be realized.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-7, 18/1-7, 19 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Ichikawa et al. (USP-5,793,724).

Regarding claims 1-3, Ichikawa et al. discloses a buffer memory address translation device. See figures 7 & 18. "Ring buffer controller 730 assigns a write address, write pointer WP, in ring buffer memory 702 corresponding to the address of the detected sector number provided by sector detector 718" (col. 7, lines 4-7). "If sector detector 718

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does not detect an address or if the detected addresses are not successive, sector detector 718 generates a sector number abnormal signal which is supplied to track jump detector 724 via ring buffer controller 730" (col. 6, lines 64-67). In an embodiment of the invention described with reference to figure 18, the sector detector or "SBCD circuit 1810 recognizes the beginning of a sector of data recorded on optical disc 104 based on the type and continuity of [frame] sync codes..." (col. 14, lines 40-42). Accordingly, Ichikawa et al. discloses the claimed analysis means (718, 1810) of analyzing a synchronization pattern included in data read from an optical disk medium 104 and positional data allowing a data position to be recognized included in the data read from the optical disk medium 104. Further, Ichikawa et al. discloses the claimed address generation means 730 of generating an address for storage into a buffer memory 702 based on a result of the analysis, wherein the read data is stored in a region corresponding to the generated address in the buffer memory 702 as claimed.

Regarding claims 4, 6, & 7, Ichikawa et al. discloses that the analysis means 1810 (fig. 18) comprises: sector address information readout means of reading sector address information (ID) included in the data read from the optical disk medium; sector address information (ID) reliability determination means of determining the reliability of the read sector address information (ID) (see col. 17, line 50, through col. 18, line 18); sector address information (ID) interpolation means of interpolating the sector address information (ID) for a sector the sector address information (ID) for which is not determined to be reliable; and sector address information (ID) selection means of selecting the address information (ID) readout means or the sector address information (ID) interpolated by the sector address information interpolation means according to a predetermined criterion (see col. 18, lines 19-23). The address generation means 730 generates an address for storage into the buffer memory 702 according to the selected sector address information (ID) as claimed.

Regarding claim 5, the read sector address information (ID) has an error detection code (IED) added thereto. See col. 14, lines 9-14. The determination of reliability is accomplished by using the added error detection code (IED) to detect an error in the read sector address information (ID) as claimed. See col. 18, lines 15-18.

Regarding claim 18/1-7, Ichikawa et al. discloses an optical disk drive, comprising: data readout means 106 of reading data from an optical disk medium 104; and a controller that, in response to a request from an external device (host CPU 1814, 732 executed to control output of data via output terminals OUT1 & OUT2 to an external device via inherent user control), controls the data readout means to temporarily store the read data into a buffer memory 702 and then transfers the same to the external device.

Regarding claims 19 & 24, as clear and understood, Ichikawa et al. discloses a "host CPU 1814 corresponding to system controller 732 (FIG. 7) [which] controls each section of apparatus 1800" (col. 12, lines 16-

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18). The host CPU (claimed "computer") inherently executes a program stored on a medium, e.g., RAM, ROM, etc., as claimed.

Claim 8 is allowed.

Claim 18 would be allowable if amended to depend only from allowed claim 8.

The following is an examiner's statement of reasons for allowance: the prior art of record considered as a whole fails to teach or suggest a buffer memory address translation device, characterized in that the buffer memory address translation device comprises: readout means of reading a frame synchronization code added to data read from an optical disk medium; storage means of encoding the read frame synchronization codes and sequentially storing the same therein; frame position digitization means of digitizing a position of a frame on an arrangement of the codes stored in the storage means; continuity determination means of determining whether the digitized frame positions are continuous; counter means of counting the number of the digitized frame positions that are determined to be continuous; **frame position determination means of comparing the number of the continuous frame positions counted by the counter means with a threshold that can be set by an external control means and, if the result of the comparison satisfies a predetermined condition, determining that the value digitized by the frame position digitization means is a frame position; frame position interpolation means of, if the condition is not satisfied in the frame position determination means, carrying out interpolation based on a previous frame position for which the condition is satisfied to find a frame position;** and address generation means of generating an address for storage into a buffer memory based on the frame position found by the frame position interpolation means or the frame position determined by the frame position determination means, and the read data is stored in a region corresponding to the generated address in the buffer memory. (bold language emphasized)

Any inquiry concerning this communication should be directed to Paul Huber at telephone number 571-272-7588.



Paul Huber  
Primary Examiner  
Art Unit 2653

pwh  
July 12, 2005